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Motorola Semiconductor Application Note

AN1760

Interfacing the AD8402 Digital Potentiometer to the MC68HC705J1A

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Introduction

The digital potentiometer (DP) allows many of the applications of mechanical trimming potentiometers to be replaced by a solid-state solution. The digital potentiometer has several benefits over a mechanical potentiometer, including compact size, freedom from shock or vibration, and the ability to withstand oil, dust, temperature extremes, and moisture.

The interface of a DP allows it to be electronically controlled by a microprocessor or microcontroller so that the user can adjust system parameters quickly and precisely. Also, automatic system initialization and calibration at the point of manufacture can be provided to increase accuracy and timeliness on the production line.

Some DP applications are:

- Volume control and panning
- LCD (liquid crystal display) contrast control
- Automatic gain control
- Programmable filters, delays, and time constants
- Power supply adjustment

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Two major configurations of the DP include the rheostat (2-terminal configuration) and the potentiometer divider (3-terminal configuration).

This application note describes the interface between the MC68HC705J1A (J1A) and Analog Devices, Inc.'s AD8402 to create these configurations for various analog circuits. Since the J1A does not have a serial module on chip, a software I/O (input/output) driver is created to provide the appropriate serial bus signals to the AD8402.

Circuitry and example code are given to demonstrate the interface between the two parts.

AD8402 Overview

The AD8402 is a member of a series of digital potentiometers. This family consists of one, two, or four potentiometers. These are the AD8400, AD8402, and AD8403. This application note utilizes the AD8402 with a 50-kΩ fixed resistance per potentiometer.

Features

The AD8400 series of digital potentiometers provides these features:

- 256-position variable resistors
- Replaces one, two, or four mechanical potentiometers
- Devices are available in resistance values of 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ
- Power shutdown mode consumes less than 5 μA
- 3-wire SPI-compatible serial bus interface
- Midscale preset on device power-up
- +2.7 volt to +5.5 volt single-supply operation
- 8/14/24-pin DIP (dual in-line), 8/14/24-pin SOIC (small outline integrated circuit), and 14/24-pin TSSOP packages

Description

The AD8400 series provides 256-position digitally controlled variable resistors (VR). The VR is designed with a fixed resistor value that has a wiper contact that taps the resistor at a point that is determined by an 8-bit digital code. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code latched into the VR. Each VR offers a programmable resistance between the A terminal and the wiper and the B terminal and the wiper. A unique switching circuit minimizes the inherent glitch found in traditional switched resistor designs by avoiding any make-before-break or break-before-make operation.

Each VR has its own latch to hold the 8-bit digital value defining the wiper position. These latches are updated from a 3-wire SPI (serial peripheral interface). Ten bits make up the data word needed for the serial input register. The first two address bits select a VR to modify and are then followed by eight data bits for the VR latch. The bits are clocked on the rising edge of the serial clock MSB (most significant bit) first. The $\overline{CS}$ pin starts a serial transaction by going low and then latches the 10 bits of data clocked by going back high.

The AD8402 provides system enhancements such as VR reset and VR shutdown. When the $\overline{RS}$ pin goes low, the values of the VR latches reset to a midscale value of $80. When the $\overline{SHDN}$ pin goes low, the part forces the resistor to an end-to-end open circuit on the A terminal and shorts the B terminal to the wiper. While in shutdown mode, the VR latches can be updated to new values. These changes will be active when the $\overline{SHDN}$ pin goes back high.

AD8402 Hardware Interface

Pinout and Pin Descriptions

Figure 1 and **Table 1** illustrate and describe the AD8402 pinout.

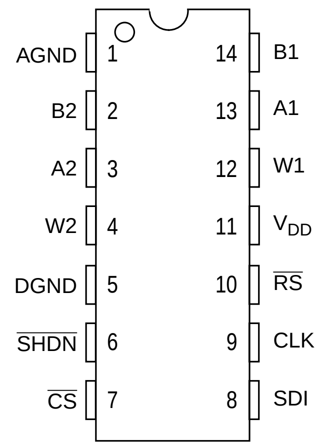

Figure 1. AD8402 Pinout

Table 1. AD8402 Pin Descriptions

Pin	Symbol	Name	I/O/PWR	Description
1	AGND	Analog ground	PWR	Analog ground; must be connected to DGND
2	B2	B2 terminal	I/O	Terminal B for VR #2
3	A2	A2 terminal	I/O	Terminal A for VR #2
4	W2	W2 wiper	I/O	Wiper for VR #2
5	DGND	Digital ground	PWR	Ground pin for digital circuitry
6	$\overline{\text{SHDN}}$	Shutdown	I	Shutdown controls VR1, VR2; makes terminal A an open circuit
7	$\overline{\text{CS}}$	Chip select	I	Selects the AD8042; when the $\overline{\text{CS}}$ pin goes high, the serial input register is decoded and the VR data is loaded
8	SDI	Serial data	I	Input pin for the serial interface
9	CLK	Serial clock	I	Clock pin for the serial interface, positive edge triggered
10	$\overline{\text{RS}}$	Reset	I	When RS goes low, VRs are reset to a midscale reading of $80
11	V_{DD}	Power	PWR	Positive power supply; specified for operation at +3 V and +5 V

Table 1. AD8402 Pin Descriptions (Continued)

Pin	Symbol	Name	I/O/PWR	Description
12	W1	W1 wiper	I/O	Wiper for VR #1
13	A1	A1 terminal	I/O	Terminal A for VR #1
14	B1	B1 terminal	I/O	Terminal B for VR #1

Block Diagram

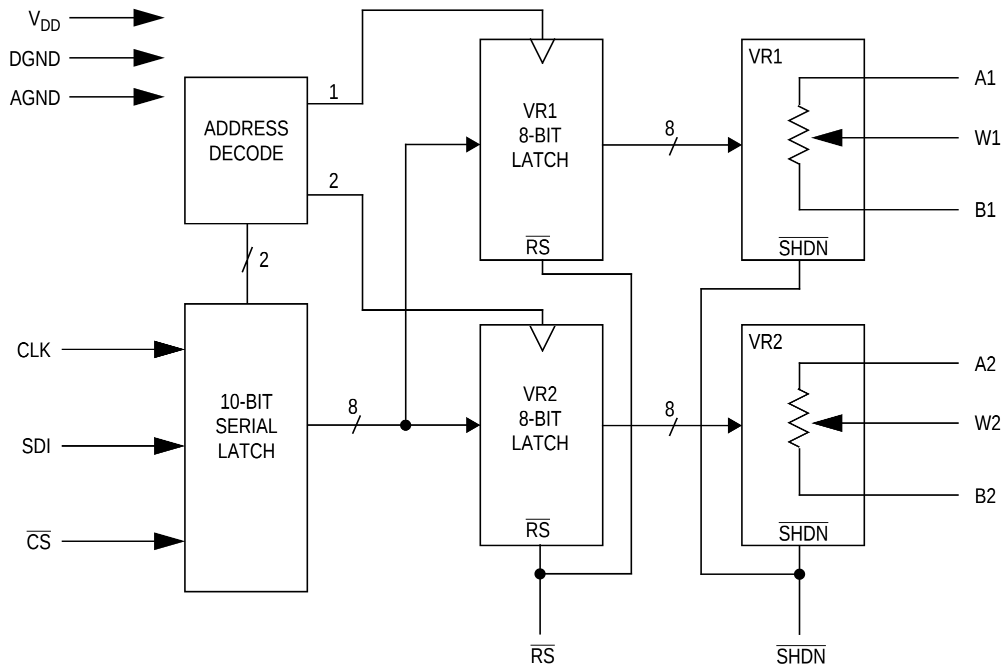

Figure 2. AD8402 Block Diagram

Serial Bus Timing

The serial port interface for the AD8402 is shown in **Figure 3**. Only logic levels are shown. Consult the AD8402 data sheet if detailed AC electrical characteristics are needed.

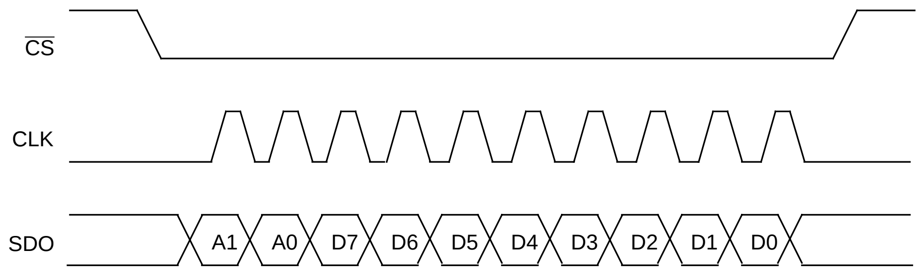

Figure 3. Serial Data Timing

Table 2 is the logic truth table that describes the interaction among the CLK, $\overline{\text{CS}}$, $\overline{\text{RS}}$, and $\overline{\text{SHDN}}$ pins.

Table 2. Control Truth Table

CLK	$\overline{\text{CS}}$	$\overline{\text{RS}}$	$\overline{\text{SHDN}}$	Register Activity
0	0	1	1	No SR effect; enables SDO pin
Positive edge	0	1	1	Shift a bit in from SDI pin
X	Positive edge	1	1	Load SR data into addressed VR latch
X	1	1	1	No operation
X	X	0	1	Sets all VR latches to midscale reading of $80
X	1	Positive edge	1	Latches all VR latches to $80
X	1	1	0	Open circuits all A terminals, connects wiper to B terminal

AD8402 Software Interface

Data Format

The serial interface requires data to be in the format shown in **Figure 4**. First, the address bits of A1 and A0 must be sent. For the single channel AD8400, A1 = A0 = 0. For the dual channel AD8402 which is used in this application note, A1 = 0.

The next eight bits are the data value to be latched into the VR.

VR ADDR		VR DATA							
B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB	LSB	MSB							LSB

Figure 4. Data Format

Programming the Variable Resistor

The nominal resistance, R_{AB}, between terminals A and B of the AD8402 used in this application note is 50 kΩ. The R_{AB} of the VR has 256 resistive contact points that can be accessed by the wiper terminal plus the B terminal contact.

For an 8-bit value of \$00, the wiper starts at the B terminal. The B terminal has an inherent resistance of 50 Ω. The next resistive connection has a digital value of \$01. It has a value equal to the B terminal resistance plus an LSB resistor value.

For the 50-kΩ part that is used, this LSB amount is equal to 50 kΩ/256 or 195.3125 Ω. Therefore, the resistive value at \$01 is 245.3125 Ω (50 Ω+195.3125 Ω).

Each LSB increase moves the wiper up the resistor ladder until the last tap point is hit.

Resistive value between terminal B and the wiper can be described as:

$$R_{WB}(D) = D * (R_{AB}/256) + R_B$$

where

R_{WB} = resistance between the wiper and terminal B

D = digital value of the VR latch

R_{AB} = the nominal resistance between terminal A and B = 50 kΩ

R_B = the resistance of terminal B = 50 Ω

Table 3 illustrates this relationship.

Table 3. R_{WB} Resistance Values with R_{AB} = 50 kΩ

D_{10}	R_{WB} (Ω)	Output State
255	49,854.6875	Full scale
128	25,050	Midscale
1	245.3125	1 least significant bit (LSB)
0	50	Zero-scale

NOTE: *Note that the zero-scale value produces a resistance of 50 Ω. Care should be taken to limit the current flow between the wiper and terminal B to a maximum value of 5 mA.*

The VR is totally symmetrical. The resistance between the wiper and terminal A also produces a resistance value of R_{WA}. When setting the resistance for R_{WA}, the digital value of $00 starts the resistance setting at its maximum value. As the digital value is increased, the R_{WA} resistance decreases.

This can be described as:

$$R_{WA}(D) = (256\text{-}D) * (R_{AB}/256) + R_B$$

where

R_{WA} = resistance between the wiper and terminal A

D = digital value of the VR latch

R_{AB} = the nominal resistance between terminal A and B = 50 kΩ

R_B = the resistance of terminal B = 50 Ω

Table 4 illustrates this relationship.

Table 4. R_{WA} Resistance Values with R_{AB} = 50 kΩ

D_{10}	R_{WA} (Ω)	Output State
255	245.3125	Full scale
128	25,050	Midscale
1	49,854.6875	1 least significant bit (LSB)
0	50,050	Zero scale

Programming the Potentiometer Divider

The digital potentiometer can be easily used to generate an output voltage proportional to the voltage applied between terminals A and B. If terminal A is connected with +5 V and terminal B is connected to ground, the wiper voltage has a range of 0 V up to 1 LSB less than the +5 V. Each LSB is equal to the voltage across terminals A and B divided by 256. The wiper's output voltage can be described as;

$$V_W(D) = (D/256) * V_{AB} + V_B$$

where

V_W = voltage on wiper

D = digital value of the VR latch

V_{AB} = voltage across terminal A and B

V_B = voltage at terminal B

Digital Potentiometer Applications

Many applications can utilize the digital potentiometer to replace traditional mechanical resistors. When using the AD8042, certain boundary conditions must be observed for proper operation.

First, all analog signals must remain within the 0 to V_{DD} range used to supply the AD8042. If the potentiometer divider circuit is driving a low-impedance load, buffer the wiper with a rail-to-rail op amp like the MC33201, OP191, or OP279.

Second, for bipolar DC applications and AC signals, a virtual ground will be needed to bias the op amp properly. For a V_{DD} of +5 V, the virtual ground must be set at 2.5 V. The connected virtual ground also must be able to sink and source current with all connected loads.

The following circuits show some basic circuits and op amp circuits implementing the digital potentiometer to program circuit parameters.

Variable Resistor

Figure 5 shows the programmable resistor or digital rheostat configuration for the AD8042.

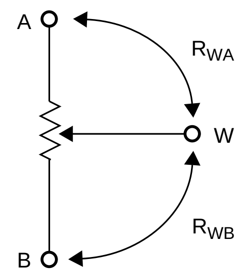

Figure 5. Programmable Resistor

Potentiometer Divider

Figure 6 shows the programmable potentiometer divider for the AD8042.

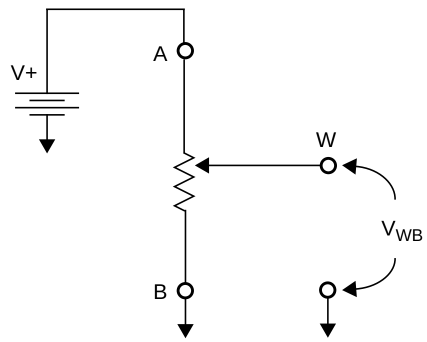

Figure 6. Programmable Potentiometer Divider

Inverting Op Amp

Figure 7 shows one channel of the AD8042 connected in an inverting programmable op amp circuit. The virtual ground is set at +2.5 volts to allow the signal to span the +/–2.5-V range. Use a rail-to-rail op amp to provide maximum output swing. When powered up, the wiper is set at its midscale position of $80.

According to the transfer function:

$$V_{Out} = -(R_{WB}/R_{WA}) * V_{In}$$

This will provide a gain of –1. As the digital value increases above its midscale position, R_{WB} increases and R_{WA} decreases. This will have an effect of amplifying the input signal. As the digital value decreases, R_{WB} decreases and R_{WA} increases and this will attenuate the signal.

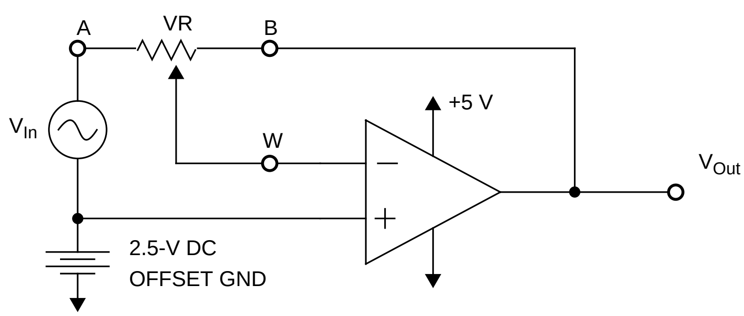

Figure 7. Programmable Inverting Op Amp

Non-Inverting Op Amp

Figure 8 shows one channel of the AD8042 connected in a non-inverting programmable op amp circuit. The virtual ground is set at +2.5 volts to allow the signal to span the +/–2.5-volt range. Use a rail-to-rail op amp to provide maximum output swing. When powered up, the wiper is set at its midscale position of $80.

According to the transfer function:

$$V_{Out} = (1+(R_{WB}/R_{WA})) * V_{In}$$

This will provide a gain of +2. As the digital value increases above its midscale position, R_{WB} increases and R_{WA} decreases. This will have an effect of amplifying the input signal. As the digital value decreases, R_{WB} decreases and R_{WA} increases and this will attenuate the signal.

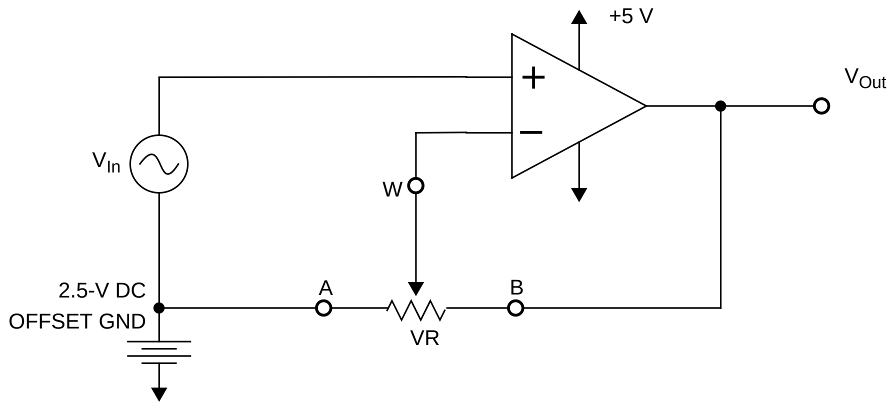

Figure 8. Programmable Non-Inverting Op Amp

Differential Op Amp

Figure 9 shows two channels of the AD8042 connected in a differential programmable op amp circuit. The virtual ground is set at +2.5 volts to allow the signal to span the +/–2.5-volt range. Use a rail-to-rail op amp to provide maximum output swing. When powered up, the wiper is set at its midscale position of $80.

According to the transfer function:

$$V_{Out} = V2_{In}*(R_{WB2}/R_{WA2}) - V1_{In}*(R_{WB1}/R_{WA1})$$

This will provide an output voltage of $V2_{In} - V1_{In}$. The resistor values can be changed as needed to provide amplification or attenuation to each input voltage.

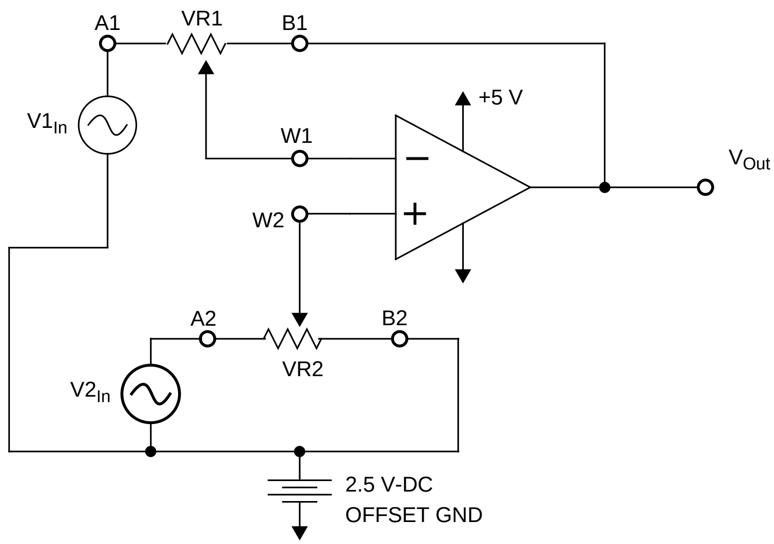

Figure 9. Programmable Differential Op Amp

Layout Considerations

Many considerations apply when laying out mixed signal designs such as the AD8042 and the MC68HC705J1A (J1A). Analog signal integrity may be greatly affected if proper layout design is not followed.

To ensure proper mixed-signal designs, use these design considerations:

- Physically separate critical analog circuits from the MCU’s digital circuits. If possible, split the board in half to separate analog and digital circuits. Each half will have its own power and ground system and will be connected at a single post.
- If possible, do not let analog lines trace cross digital lines. If this must happen, make sure they cross at right angles to each other.
- Use power or ground traces to isolate the analog-input pins from the digital pins.
- With quality ceramic capacitors, bypass the power supplies to the proper ground at the operational amplifier power pins. Keep the bypass capacitors lead lengths as short as possible.

- To bypass low-frequency power supply noise, use tantalum or aluminum electrolytic capacitors of 5 to 20 μF. These should be placed near the point the power supplies enter the board.
- If economically possible, use separate analog and digital ground planes. The two ground planes should be tied together at the low-impedance power-supply source.

MC68HC705J1A Hardware Interface

With only 20 pins, the J1A is one of the smaller members of the HC05 Family. It has a total of 1240 bytes of erasable programmable read-only memory (EPROM) and includes 14 I/O (input/output) pins. The schematic used for testing the J1A to AD8402 interface on the MMEVS development system is shown in **Figure 10**.

The pins used to drive the AD8402 on the J1A are:

- Port A, bit 0 — This I/O pin (CLK) is configured as an output to drive the serial clock pin, CLK.
- Port A, bit 1 — This I/O pin (SDO) is configured as an output to transmit data to the SDI pin.
- Port A, bit 2 — This I/O pin (CS) is configured as an output to drive the chip select pin, $\overline{CS}$.
- Port A, bit 3 — This I/O pin (RS) is configured as an output to drive the reset pin, $\overline{RS}$.

For further information on the MC68HC705J1A, consult the *MC68HC705J1A Technical Data*, Motorola document order number MC68HC705J1A/D.

The test circuit is designed to test the operation of the AD8402. VR1 can be used to test a potentiometer voltage divider. The voltage created on W1 of VR1 can be measured at TP1. VR2 can be used to test a variable potentiometer or rheostat. The resistance created on VR1 can be measured across TP2 and TP3.

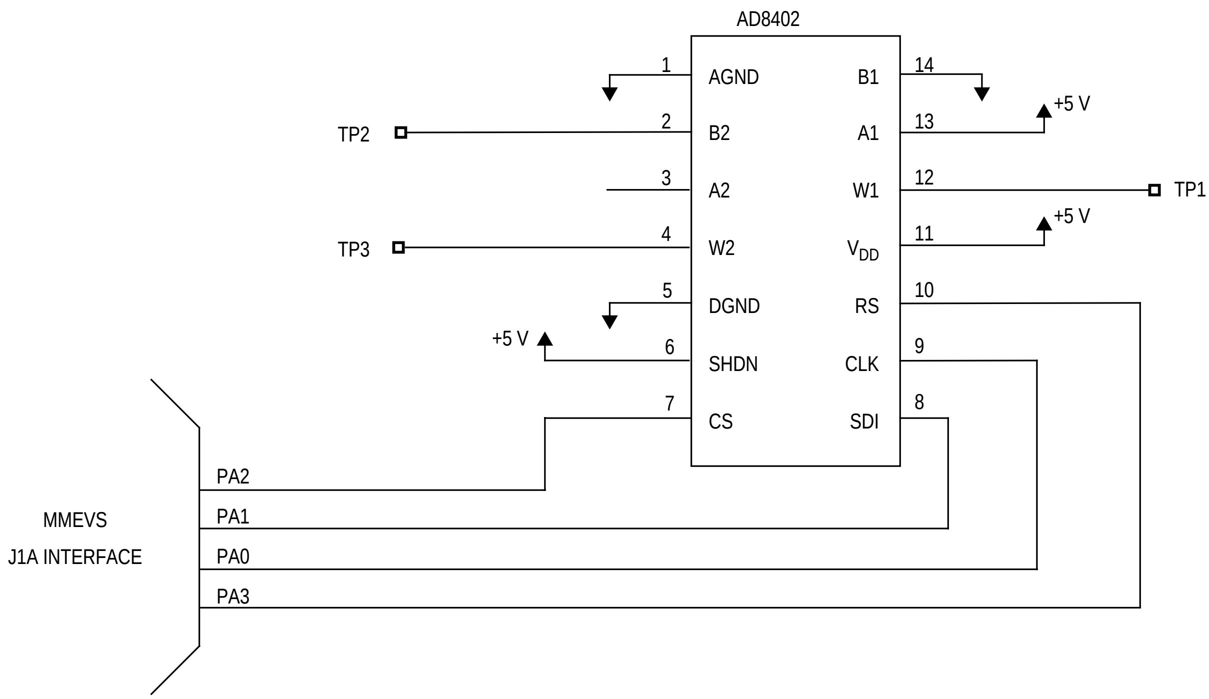

Figure 10. J1A to AD8402 Interface Test Circuit

MC68HC705J1A Test Software

The flowcharts for the I/O-driven AD8402 appear in **Figure 11** and **Figure 12**.

Figure 11 shows the flowchart for the transmit routine to the AD8402. This routine was written especially for the AD8402 and is not a full-featured representation of Motorola's SPI (serial peripheral interface) module found on other microcontrollers. Enhancements to the routine were not included to maximize the code's efficiency.

I/O driving is the process of toggling I/O pins with software instructions to emulate a certain piece of hardware peripheral. General I/O pins are used to send out the correct serial transmission protocol to the AD8402. The HC05 CPU provides special instructions to specifically manipulate single I/O pins. The AD8402 serial stream shown in **Figure 3** will be re-created by three I/O pins on the J1A.

This transmission has been put into a subroutine called TXD. The flowchart is in **Figure 11**. This subroutine is detailed here.

1. *Start the transmission* — The $\overline{CS}$ pin is written low.
2. *Initialization* — Load the X register with 10; use it as a counter.
3. *Write the serial output pin* — Bit 1 of VR_ADDR is read. If it is high, a 1 is written to the SDO pin. If it is low, a 0 is written to the SDO pin.
4. *Clock the serial clock pin* — The CLK pin is written high and then written low.
5. *Rotate VR_ADDR and VR_DATA* — Arithmetically shift left VR_DATA (C <- bit 7) then rotate left VR_ADDR (bit 0 <- C). The next bit to be sent out is now in bit 1 of VR_ADDR.
6. *Is the loop done?* — The X register is decremented and checked to see if it is 0. If X is not 0, the code is executed at the start of writing the SDO pin, step 3. This loop continues until 10 transmissions are completed.
7. *End the transmission* — The $\overline{CS}$ pin is written high and the data is latched into the AD8402. Return from subroutine.

Figure 12 shows the flowchart for the main test routine. The sequence of tests is:

1. With 5 volts on A1 and B1 connected to ground, create 1.25 volts on W1. Test the voltage at TP1.
2. Reset the AD8402. The voltage at TP1 should now read 2.5 V.
3. With A2 open, create a ~10-kΩ resistance on VR2. Measure this resistance across TP2 and TP3.
4. Create a ramping voltage waveform on TP1. Using an oscilloscope, verify that the waveform ramps from 0 volts to 5 volts.

The assembly code for the test routine is provided in **Code Listing**.

Development Tools

The interface was created and tested using these development tools:

- M68MMPFB0508 — Motorola MMEVS platform board
- M68EM05J1A — Motorola J1A emulation module
- Win IDE Version 1.02 — Editor, assembler, and debugger by P&E Microcomputer Systems, Inc.

References

MC68HC705J1A Technical Data, Motorola document order number MC68HC705J1A/D, 1996.

M68HC05 Applications Guide, Motorola document order number M68HC05AG/AD, 1996.

AD8402 Datasheet, Analog Devices, Inc., 1997.

HC05/08 Website:

http://design-net.com/csic/welcome.htm

Development Tools Website:

http://design-net.com/csic/devsys/sg173/sg173.htm

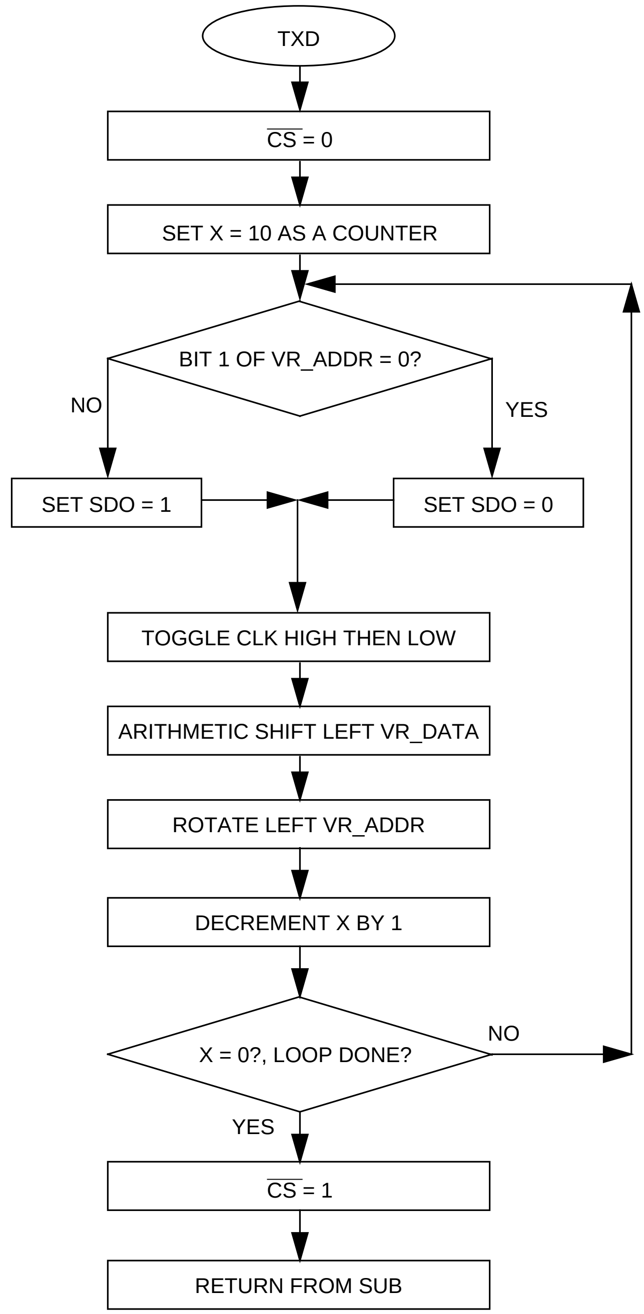

Figure 11. Serial Driver Flowchart

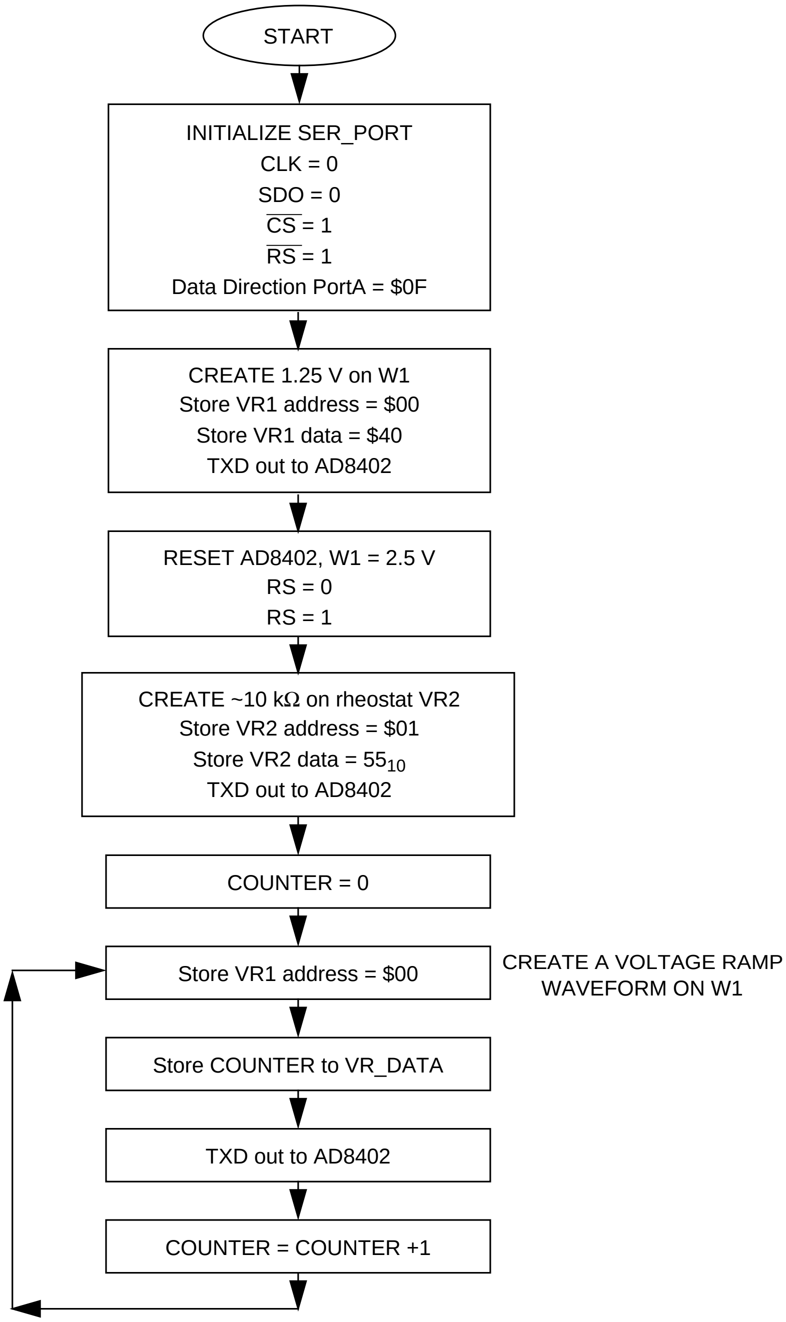

Figure 12. Main Test Routine Flowchart

Code Listing

```
*********************************************************************************
*
* File name: AD8402.ASM
* Example Code for the MC68HC705J1A Interface to the
*     Analog Devices Digital Potentiometer
* Ver: 1.0
* Date: June 23, 1998
* Author: Mark Glenewinkel
*         Motorola Field Applications
*         Consumer Systems Group
* Assembler: P&E IDE ver 1.02
*
* For code explanation and flow charts,
* please consult Motorola Application Note
*    “Interfacing the AD8402 Digital Potentiometer to the MC68HC705J1A”
*    Literature order number AN1760/D
*
*********************************************************************************

*** SYSTEM DEFINITIONS AND EQUATES ***********************************************
*** Internal Register Definitions
PORTA          EQU      $00                 ;PortA
DDRA           EQU      $04                 ;data direction for PortA

*** Application Specific Definitions
SER_PORT       EQU      $00                 ;PortA is SER_PORT
SDO            EQU      1T                  ;PortA, bit 0, data signal
CLK            EQU      0T                  ;PortA, bit 1, clock signal
CS             EQU      2T                  ;PortA, bit 2, chip select
RS             EQU      3T                  ;PortA, bit 3, reset signal

VR1            EQU      0T                  ;address for VR1
VR2            EQU      1T                  ;address for VR2


*** Memory Definitions
EPROM          EQU      $300                ;start of EPROM mem
RAM            EQU      $C0                 ;start of RAM mem
RESET          EQU      $7FE                ;vector for reset


*** RAM VARIABLES ****************************************************************
               ORG      RAM
VR_ADDR        DB       $00                 ;storage for addr to be sent
VR_DATA        DB       $00                 ;storage for data to be sent
COUNTER        DB       $00                 ;temp counter
```

```
*** MAIN ROUTINE *******************************************************************
                ORG      EPROM               ;start at beginning of EPROM
*** Initialize Ports
START           bclr     CLK,SER_PORT        ;CLK=0
                bclr     SDO,SER_PORT        ;SDO=0
                bset     CS,SER_PORT         ;CS=1
                bset     RS,SER_PORT         ;RS=1

                lda      #%00001111          ;make SER_PORT pins outputs
                sta      DDRA

*** Create 1.25V on W1
                lda      #VR1
                sta      VR_ADDR             ;address VR1
                lda      #$40
                sta      VR_DATA             ;1/4 of voltage range
                jsr      TXD                 ;send address and data

*** Reset AD8402, W1=2.5V
                bclr     RS,SER_PORT         ;RS=0
                bset     RS,SER_PORT         ;RS=1

*** Create a ~10K ohm reading on rheostat VR2
                lda      #VR2
                sta      VR_ADDR             ;address VR2
                lda      #51T
                sta      VR_DATA             ;1/5 of resistor change
                jsr      TXD                 ;send address and data

*** Create a voltage ramp waveform on W1
                clr      COUNTER             ;COUNTER=0
RAMP_LOOP       lda      #VR1
                sta      VR_ADDR             ;address VR1
                lda      COUNTER
                sta      VR_DATA             ;data=COUNTER
                jsr      TXD                 ;send address and data
                inc      COUNTER             ;COUNTER=COUNTER+1
                bra      RAMP_LOOP           ;infinite loop
```

```
 ************************************************************************************
*** Routine takes contents of VR_ADDR and VR_DATA and sends
*** them out to the AD8402, MSB first
*** VR_ADDR and VR_DATA are destroyed
TXD            bclr     CS,SER_PORT         ;CS=0

               ldx      #10T                ;set counter

WRITE          brclr    1,VR_ADDR,CLR       ;Check bit 1 of VR_ADDR
               bset     SDO,SER_PORT        ;SDO=1
               bra      CLOCK_IT            ;branch to clock_it
CLR            bclr     SDO,SER_PORT        ;SDO=0
               brn      CLR                 ;evens it out

CLOCK_IT       bset     CLK,SER_PORT        ;CLK=1
               bclr     CLK,SER_PORT        ;CLK=0
               asl      VR_DATA             ;rotate left VR_DATA
                                            ;C=MSB of VR_DATA
               rol      VR_ADDR             ;rotate left with C
               decx                         ;decrement counter
               bne      WRITE               ;loop over?

               bset     CS,SER_PORT         ;CS=1, latch data

                        rts                 ;return from sub


*** VECTOR TABLE ******************************************
               ORG     RESET
               DW      START
```

Application Note

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